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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,968	01/29/2004	Dominique Mangelinck	ASTAP2004-01	1967

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EXAMINER	
SARKAR, ASOK K	
ART UNIT	PAPER NUMBER
2891	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/707,968	MANGELINCK ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 – 41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Gardner, US 6,100,173.

Regarding claim 1, Gardner teaches a method of fabricating a gate electrode for a semiconductor comprising the steps of:

- providing a substrate 10 (Fig. 1);
- providing a substrate prepared with a gate stack, the gate stack includes a gate dielectric 14 on the substrate and a gate layer 16 on the gate dielectric 14, the gate layer comprising a first material of thickness t_p , the first material being selected from the group consisting of Si (column 5, lines 55 – 67) ;
- providinga layer of metal 26 of thickness t (Fig. 6); and
- annealing the layers, such that substantially all of the first material of the gate material and metal of the metal layer are consumed during reaction with one another (Fig. 7) in between column 6, line 61 and column 7, line 24 to form a

resulting layer which serves as a ate electrode in contact with the gate dielectric 14 with reference to Fig. 8.

Regarding claims 2 and 25, Gardner teaches the metal Ti or Co in column 7, line 2.

Regarding claim 3, Gardner teaches the gate stack further comprises dielectric Sidewall spacers 22 and providing the metal layer comprises depositing the metal layer on the first material layer with reference to Fig. 6.

Regarding claims 4 and 5, Gardner teaches the thicknesses t_p and t_m are related by a predetermined ratio of t_m /t_p and the ratio is determined by the first material and the metal since sometimes the reaction does not consume all of the metal.

Regarding claim 6, Gardner teaches annealing is performed at temperatures ranging from 300 to 900°C in column 7, line 11.

Regarding claim 7, Gardner teaches the step of depositing a further layer of metal on the gate electrode in column 7, lines 31 – 35 to increase gate thickness with reference to Fig. 9.

Regarding claim 8, Gardner teaches forming source/drain contacts 18 simultaneously with the gate electrode with reference to Fig. 3.

Regarding claim 9, Gardner teaches as much as 5% of one of the first material and the metal remains following reaction with the other of the metal and the first material in column 7, lines 14 – 20.

Regarding claim 10, Gardner teaches the gate electrode for a semiconductor device comprising a substrate with a gate stack formed thereon, the gate stack includes

a gate dielectric on the substrate and a gate electrode on the gate dielectric , wherein the gate electrode comprises a first material and a metal, which have been substantially consumed during reaction with one another caused by annealing with reference to Figs 4 and 6 as was described earlier in rejecting claim 1.

Regarding claims 11 and 12, Gardner teaches these limitations as was described earlier in rejecting claims 1 and 2.

Regarding claim 13, Gardner teaches as much as 5% of one of the first material and the metal remains following reaction with the other of the metal and the first material as was described earlier in rejecting claim 9.

Regarding claim 14, Gardner teaches the step of depositing a layer of metal on the gate electrode as was described earlier in rejecting claim 7.

Regarding claim 15, Gardner teaches the gate electrode is incorporated in a CMOS semiconductor device in column 6, lines 25 – 36.

Regarding claims 16, 18 and 19, Gardner teaches all limitations of the claim as described earlier in rejecting claims 1 – 9. The first layer material such as polysilicon inherently have the work functions close to the mid – gap energy of semiconductor material such as silicon. The reduction of problems associated with inversion and agglomeration associated with formation of the transistor is inherent.

Regarding claim 17, Gardner teaches the substrate is prepared with at least first and second gate stacks with dielectric sidewall spacers on the substrate and first and second diffusion regions in the substrate adjacent to the gate stacks, the gate stacks include a gate dielectric on the substrate and a gate layer on the gate dielectric, the first

and second gate stacks serving as a first PMOS transistor and a first NMOS transistor to form a CMOS integrated circuit; and the material of the first layer comprises silicon as was described earlier in rejecting claims 1 and 15. The formation of two gates with two gate stacks, sidewall pacers and diffusion regions are inherent in the methods of preparing PMOS and NMOS parts of the CMOS transistor.

Regarding claims 20, 23, 27, 28, 30, 32, 34, 36, 38 and 40, Gardner teaches annealing or RTA in column 7, lines 6 – 11.

Regarding claims 21 and 24, Gardner teaches unconsumed gate layer is less than or equal to 5% and unreacted metal layer is less than or equal to 10% in column 7, lines 15 – 19.

Regarding claims 22, 26, 31, 35 and 39, Gardner teaches metal layer forms silicide over the diffusion regions with reference to Figs. 10 – 12.

Regarding claims 29 and 37, Gardner teaches the first layer comprises a first thickness t_p and the metal layer comprises a second thickness t_m, and wherein a minimum of a ratio of the first and second thickness t_p/t_m results in consumption of substantially the first gate and metal layers during processing of the metal layer as shown in Figs. 6 – 8 and associated descriptions in the disclosure.

Regarding claim 33, Gardner teaches etching remaining portion of unreacted metal layer above the gate electrode after processing the metal layer in column 7, lines 19 – 21.

Regarding claim 41, Gardner teaches an integrated circuit comprising a transistor disposed on a subsrrate, the transistor having a gate stack with a gate dielectric

disposed on the substrate and a gate electrode disposed on and in contact with the gate dielectric, and first and second diffusion regions adjacent to the gate stack, the gate electrode is formed from an amorphous or polycrystalline first layer and a metal layer which have been substantially consumed during reaction with one another caused by annealing, wherein problems associated with inversion and agglomeration associated with forraafion of the transistor is reduced with reference to Fig. 12. This is a product by process claim.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown,* 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Asok K. Sarkar
January 10, 2007

Primary Examiner